S.N. 09/955,874
Art Unit: 2819

IN THE CLAIMS:

1. Previously cancelled.

2. (Currently Amended) A phase locked loop comprising a phase comparator generating an output signal that is used to drive a voltage controlled oscillator, and a modulus N prescaler circuit coupled to an output of said voltage controlled oscillator, said prescaler circuit comprising an input node for coupling to said output of said voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N, said input signal comprising two clock input signals, an output node for outputting a frequency divided signal that is coupled to said phase comparator, and a plurality of divider stages coupled between the input node and the output node for dividing the input signal by N, and further comprising at least one resampling stage coupled to an output of at least one of said divider stages for receiving an output signal therefrom, said output signal comprising two output signals, and for synchronizing edges of the output signal to edges of the input signal, thereby reducing temporal ambiguity in the occurrence of the edges of the output signal, where said at least one resampling stage is comprised of a flip-flop having a data input coupled to said output of said at least one of said divider stages and a clock input coupled to said input node for being clocked with said output of said voltage controlled oscillator.

3. (Original) A phase locked loop as in claim 2, wherein the value of N is programmable.

4. (Previously Amended) A phase locked loop as in claim 2, wherein said flip-flop is comprised of a D-type flip-flop.

5. (Currently Amended) A method for reducing power consumption in a frequency source of a mobile station, comprising:

operating a phase locked loop as part of the frequency source to generate a signal having

a desired frequency, the step of operating the phase locked loop including a step of dividing a frequency of an output signal of a voltage controlled oscillator by a predetermined amount to generate a frequency divided signal, the output signal of the voltage controlled oscillator comprising two output clock signals; and

resampling the frequency divided signal using a flip-flop circuit that has a data input coupled to said frequency divided signal, the frequency divided signal comprising two frequency divided signals, and a clock input that is clocked with the output signal of the voltage controlled oscillator to reduce jitter in the frequency divided signal.

6. (Original) A method as in claim 5, wherein the step of resampling operates a modulus N prescaler circuit that is coupled to the output of the voltage controlled oscillator, the prescaler circuit comprising an input node for coupling to the output of the voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N, an output node for outputting a frequency divided signal that is coupled to a phase comparator of the phase locked loop, and a plurality of the frequency divider circuits coupled between the input node and the output node for dividing the input signal by N, where the step of resampling is accomplished in a resampling stage coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal, thereby reducing jitter of the output signal.

7. (Original) A method as in claim 6, wherein the value of N is programmable.

8. (Previously Amended) A method as in claim 6, wherein the flip-flop circuit is comprised of a D-type flip-flop.

9. (Currently Amended) A method to operate a phase locked loop as part of a frequency source to generate a signal having a desired frequency, comprising:

operating a multi-modulus prescaler function of the phase locked loop to divide a frequency of an output signal of an oscillator by a predetermined amount to generate a frequency-divided signal, the output signal of the oscillator comprising two output clock signals; and

resampling the frequency divided signal using a flip-flop circuit that has a data input coupled to the frequency divided signal and a clock input that is clocked with the output signal of the oscillator, the frequency divided signal comprising two frequency divided signals.

10. Previously cancelled.

11. (Currently Amended) A method as in claim 9, wherein the step of resampling operates a prescaler circuit that is coupled to the output of the oscillator, the prescaler circuit comprising an input node for coupling to the output of the oscillator for receiving an input signal having a characteristic frequency to be divided by N, the input signal being the output signal of the oscillator that comprises the two output clock signals, an output node for outputting a the frequency divided signal that is coupled to a phase comparator of the phase locked loop, and a plurality of the frequency divider circuits coupled between the input node and the output node for dividing the input signal by N, where the step of resampling is accomplished in a resampling stage coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal, thereby equalizing the delay added in different modes of the multi-modulus prescaler function..

12. (Original) A method as in claim 11, wherein the value of N is programmable.

13. (Previously Amended) A method as in claim 9, where said flip-flop is comprised of a D-type flip-flop that is clocked with the output signal of the oscillator.

14. Cancelled

15. (Original) A method as in claim 9, wherein the steps of operating and resampling are performed while a mobile station is tuned to a desired RF frequency band.

16. (Original) A method as in claim 9, wherein the output frequency of the oscillator is set in accordance with an output of a control device of a mobile station.

17. (Currently Amended) A mobile station, comprising a radio frequency (RF) transceiver that is tunable using a frequency synthesizer that comprises a phase lock loop (PLL), said PLL comprising a phase comparator for comparing a frequency divided oscillator output signal to a frequency divided voltage controlled oscillator (VCO) output signal and generating in accordance with said comparison a control signal that is applied via a loop filter to said VCO, further comprising a prescaler block disposed between an output of said VCO and an input of a frequency divider, said prescaler block comprising a frequency divider block having an input coupled to said output of said VCO, the output of the VCO comprising two output clock signals, said frequency divider block having an output for outputting a frequency divided signal, said prescaler block further comprising a flip-flop having an input coupled to said output of said frequency divider block and a clock input coupled to said output of said VCO, the output of said frequency divider block comprising two frequency divided output signals, said flip-flop operating to cause said prescaler block to output to said frequency divider a prescaled VCO signal having edge transitions that are synchronized to edge transitions of the VCO output signal.

18. (Previously Added) A mobile station as in claim 17, where said prescaler comprises a multi-modulus prescaler.

19. (Previously Added) A mobile station as in claim 17, where said prescaler comprises a phase rotation modulus prescaler.

20. (Previously Added) A mobile station as in claim 17, where said RF transceiver comprises a direct conversion receiver.

21. (Previously Added) A mobile station as in claim 17, where said PLL is used when at least one of tuning from one RF frequency channel to another, and tuning from one RF frequency band to another.